

DDR2 SDRAM SORDIMM

MT9HTF6472RH – 512MB

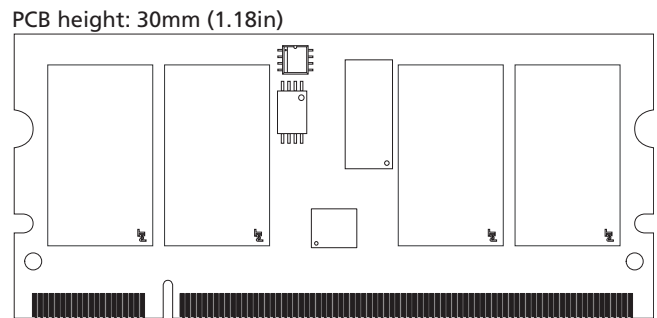
MT9HTF12872RH – 1GB

For component data sheets, refer to Micron’s Web site: www.micron.com

Features

- 200-pin, small-outline registered dual in-line memory module (SORDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 512MB (64 Meg x 72) and 1GB (128 Meg x 72)
- Supports ECC error detection and correction
- VDD = VDDQ = +1.8V
- VDDSPD = +3.0V to +3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 t_{CK}
- Programmable burst lengths (BL) 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- PLL to reduce system clock line loading
- Gold edge contacts
- Single rank
- I²C temperature sensor

Figure 1: 200-Pin SORDIMM (MO-224)



Options

- Operating temperature¹
 - Commercial (0°C ≤ T_A ≤ +70°C)
 - Industrial (-40°C ≤ T_A ≤ +85°C)
- Package
 - 200-pin DIMM (Pb-free)
- Frequency/CAS latency²
 - 2.5ns @ CL = 5 (DDR2-800)
 - 2.5ns @ CL = 6 (DDR2-800)
 - 3.0ns @ CL = 5 (DDR2-667)
 - 3.75ns @ CL = 4 (DDR2-533)³

Marking

None
I
Y
-80E
-800
-667
-53E

- Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
3. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				t _{RCD} (ns)	t _{RP} (ns)	t _{RC} (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55



512MB, 1GB (x72, ECC, SR) 200-Pin DDR2 SDRAM SORDIMM Features

Table 2: Addressing

Parameter	512MB	1GB
Refresh count	8K	8K
Row address	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	8 (BA0–BA2)
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M8,¹ 512Mb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT9HTF6472RHY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472RHY-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472RHY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472RHY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

Table 4: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M8,¹ 1Gb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT9HTF12872RHY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872RHY-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872RHY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872RHY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.
Example: MT9HTF12872RHY-667E1.



Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SORDIMM Front								200-Pin SORDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQ18	101	VDD	151	Vss	2	Vss	52	Vss	102	A6	152	Vss
3	DQ0	53	DQ19	103	A5	153	DQS5#	4	DQ4	54	DQ28	104	A4	154	DM5
5	Vss	55	Vss	105	A3	155	DQS5	6	DQ5	56	DQ29	106	VDD	156	Vss
7	DQ1	57	DQ24	107	A2	157	Vss	8	Vss	58	Vss	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	VDD	159	DQ42	10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	Vss	111	A10	161	DQ43	12	Vss	62	Vss	112	BA1	162	Vss
13	Vss	63	DQS3#	113	BA0	163	Vss	14	DQ6	64	DQ30	114	VDD	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48	16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	Vss	117	VDD	167	DQ49	18	Vss	68	Vss	118	S0#	168	Vss
19	Vss	69	DQ26	119	CAS#	169	Vss	20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	NC	171	DQS6#	22	DQ13	72	CB5	122	A13	172	Vss
23	DQ9	73	Vss	123	VDD	173	DQS6	24	Vss	74	Vss	124	VDD	174	DQ54
25	Vss	75	CB0	125	NC	175	Vss	26	DM1	76	DM8	126	CK0	176	DQ55
27	DQS1#	77	CB1	127	NC	177	DQ50	28	Vss	78	Vss	128	CK0#	178	Vss
29	DQS1	79	Vss	129	DQ32	179	DQ51	30	DQ14	80	CB6	130	Vss	180	DQ60
31	Vss	81	DQS8#	131	Vss	181	Vss	32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56	34	Vss	84	Vss	134	DQ37	184	Vss
35	DQ11	85	Vss	135	DQS4#	185	DQ57	36	DQ20	86	CB2	136	Vss	186	DM7
37	Vss	87	CKE0	137	DQS4	187	Vss	38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	NC	139	Vss	189	DQS7#	40	Vss	90	Vss	140	Vss	190	Vss
41	DQ17	91	EVENT#	141	DQ34	191	DQS7	42	RESET#	92 ¹	NC/BA2	142	DQ38	192	DQ63
43	Vss	93	VDD	143	DQ35	193	DQ58	44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	Vss	195	Vss	46	Vss	96	A11	146	Vss	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59	48	DQ22	98	VDD	148	DQ44	198	SA1
49	Vss	99	A7	149	DQ41	199	VDDSPD	50	DQ23	100	A8	150	DQ45	200	SA0

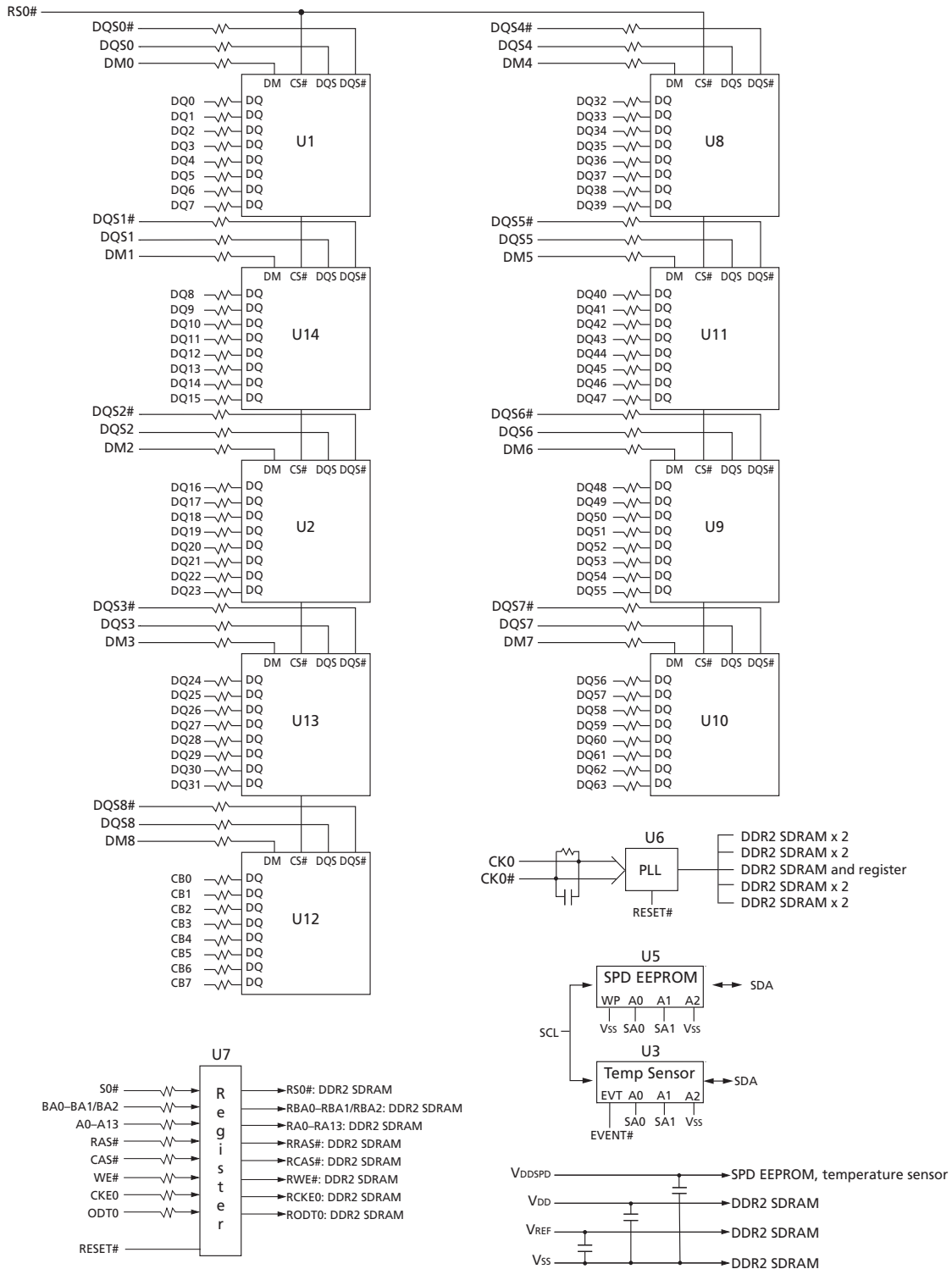
Notes: 1. Pin 92 is NC for 512MB and BA2 for 1GB.

Table 6: Pin Descriptions

Symbol	Type	Description
A0–A13	Input (SSTL_18)	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA0–BA2	Input (SSTL_18)	Bank address inputs: BA0–BA1/BA2 define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0, BA1 (512MB), BA0–BA2 (1GB).
CK0, CK0#	Input (SSTL_18)	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL_18)	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
DM0–DM8	Input (SSTL_18)	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODT0	Input (SSTL_18)	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input (SSTL_18)	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	Reset: Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
S0#	Input (SSTL_18)	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA1	Input	Presence-detect address inputs: These pins are used to configure the presence-detect and temperature sensor devices.
SCL	Input	Serial clock: SCL is used to synchronize the presence-detect and temperature sensor data transfer to and from the module.
CB0–CB7	I/O (SSTL_18)	Check bits.
DQ0–DQ63	I/O (SSTL_18)	Data input/output: Bidirectional data bus.
DQS0–DQS8 (DQS0#–DQS8#)	I/O (SSTL_18)	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O (SSTL_18)	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect and temperature sensor devices.
EVENT#	Output	Temperature sensor alarm output: The event pin is used to flag critical module temperatures.
VDD	Supply	Power supply: +1.8V ±0.1V.
VDDSPD	Supply	Serial EEPROM and temperature sensor positive power supply: +3.0V to +3.6V.
VREF	Supply	SSTL_18 reference voltage (V _{DD} /2).
VSS	Supply	Ground.
NC	–	No connect: These pins are not connected on the module.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT9HTF6472RH and MT9HTF12872RH DDR2 SDRAM modules are high-speed, CMOS, dynamic random access 512MB and 1GB memory modules organized in a x72 configuration. These modules use a 512Mb DDR2 SDRAM device with four internal banks or a 1Gb DDR2 SDRAM device with eight internal banks.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

These DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. The EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is tied to Vss on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	
VDD	VDD supply voltage relative to Vss	-0.5	+2.3	V	
VIN, VOUT	Voltage on any pin relative to Vss	-0.5	+2.3	V	
II	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	-5	+5	μA
		CK0, CK0#	-250	+250	
		DM	-5	+5	
IOZ	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQ and ODT are disabled	-5	+5	μA	
IVREF	VREF leakage current; VREF = valid VREF level	-18	+18	μA	
TA	Module ambient operating temperature	Commercial	0	+70	$^{\circ}C$
		Industrial	-40	+85	$^{\circ}C$
TC ¹	DDR2 SDRAM component case operating temperature ²	Commercial	0	+85	$^{\circ}C$
		Industrial	-40	+95	$^{\circ}C$

- Notes: 1. Refresh rate is required to double when $85^{\circ}C < T_C \leq 95^{\circ}C$.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E

IDD Specifications

Table 9: DDR2 IDD Specifications and Conditions – 512MB

Values are shown for the MT47H64M8 DDR2 SDRAM only and are computed from the values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	Units	
Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	900	810	720	mA	
Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	1,035	945	855	mA	
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	63	63	63	mA	
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	450	405	360	mA	
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	495	450	405	mA	
Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3Pf	360	315	270	mA
	Slow PDN exit MR[12] = 1	IDD3Ps	108	108	108	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	630	585	495	mA	
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1,755	1,530	1,260	mA	
Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1,845	1,620	1,305	mA	
Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	2,070	1,620	1,530	mA	
Self refresh current: CK and CK# at 0V; CKE $\leq 0.2\text{V}$; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	63	63	63	mA	
Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7	2,700	2,160	2,025	mA	



512MB, 1GB (x72, ECC, SR) 200-Pin DDR2 SDRAM SORDIMM Electrical Specifications

Table 10: DDR2 IDD Specifications and Conditions – 1GB

Values are shown for the MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition	Symbol	-80E/ -800	-667	-53E	Units	
Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	810	765	630	mA	
Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	990	900	855	mA	
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	63	63	63	mA	
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	450	360	360	mA	
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	450	360	360	mA	
Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3Pf	360	270	270	mA
	Slow PDN exit MR[12] = 1	IDD3Ps	90	90	90	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	540	495	405	mA	
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1,440	1,215	1,125	mA	
Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1,440	1,215	1,125	mA	
Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	2,115	1,935	1,890	mA	
Self refresh current: CK and CK# at 0V; CKE $\leq 0.2\text{V}$; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	63	63	63	mA	
Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (IDD), AL = RCD (IDD) - 1 $\times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7	3,015	2,520	2,430	mA	

Register and PLL Specifications

Table 11: Register Specifications
SSTU32872 devices or equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH(DC)}	Address, control, command	SSTL_18	V _{REF(DC)} + 125	V _{DDQ} + 250	mV
DC low-level input voltage	V _{IL(DC)}	Address, control, command	SSTL_18	0	V _{REF(DC)} - 125	mV
AC high-level input voltage	V _{IH(AC)}	Address, control, command	SSTL_18	V _{REF(DC)} + 250	V _{DD}	mV
AC low-level input voltage	V _{IL(AC)}	Address, control, command	SSTL_18	0	V _{REF(DC)} - 250	mV
Output high voltage	V _{OH}	Parity output	SSTL_18	1.2	–	V
Output low voltage	V _{OL}	Parity output	SSTL_18	–	0.5	V
Input current	I _I	All pins	V _I = V _{DDQ} or V _{SSQ}	–5	+5	μA
Static standby	I _{DD}	All pins	RESET# = V _{SSQ} (I _O = 0)	–	200	μA
Static operating	I _{DD}	All pins	RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _O = 0	–	80	mA
Dynamic operating (clock tree)	I _{DDD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	μA
Dynamic operating (per each input)	I _{DDD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _O = 0; CK and CK# switching 50% duty cycle; One data input switching at ^t _{CK/2} , 50% duty cycle	–	Varies by manufacturer	μA
Input capacitance (per device, per pin)	C _I	All inputs except RESET#	V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C _I	RESET#	V _I = V _{DDQ} or V _{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 12: PLL Specifications
CUA845 device or JEDEC82-21 equivalent

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH}	OE, OS, CK, CK#	LVC MOS	0.65 × V _{DD}	–	V
DC low-level input voltage	V _{IL}	OE, OS, CK, CK#	LVC MOS	–	0.35 × V _{DD}	V
Input voltage (limits)	V _{IN}	–	–	–0.3	V _{DD} + 0.3	V
Input differential-pair cross voltage	V _{IX}	–	Differential input	(V _{DD} /2) - 0.15	(V _{DD} /2) + 0.15	V
Input differential voltage	V _{ID(DC)}	–	Differential input	0.3	V _{DD} + 0.4	V
Input differential voltage	V _{ID(AC)}	–	Differential input	600	V _{DD} + 0.4	V
Input current	I _I	OE, OS, FBIN, FBIN#	V _I = V _{DD} or V _{SS}	–10	10	μA
		CK, CK#	V _I = V _{DD} or V _{SS}	–250	+250	μA
Output disabled current	I _{ODL}	–	OE = L, V _{ODL} = 100mV	100	–	μA
Static supply current	I _{DDL}	–	CL = 0pf	–	500	μA
Dynamic supply	I _{DD}	n/a	CK and CK# = 410 MHz all output are open (not connected to a PCB)	–	300	mA
Input capacitance	C _{IN}	Each input	V _I = V _{DD} or V _{SS}	2	3	pF

Table 13: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	t _L	–	6	μs
Input clock slew rate	slr(i)	1	4	V/ns
SSC modulation frequency	–	30	33	kHz
SSC clock input frequency deviation	–	0.0	–0.5	%
PLL loop bandwidth (–3dB from unity gain)	–	2	–	MHz

- Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Temperature Sensor

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I²C bus shared with the SPD. This sensor complies with the "Mobile Platform Memory Module Thermal Sensor Component Specification," which is found in JEDEC standard JESD21-C.

Table 14: Temperature Sensor Specifications

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	VDD	+3.0	+3.6	V
Average operating supply current	–	–	+500	μA
Input high voltage: Logic 1; All inputs	V _{IH}	+2.1	–	V
Input low voltage: Logic 0; All inputs	V _{IL}	–	+0.8	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	–	+0.4	V
Logic input current	I _{IH}	–5.0	+5.0	μA
	I _{IL}	–5.0	+5.0	μA
Temperature sensing range	–	–40	+125	°C

Table 15: Temperature Sensor AC Timing

Parameter/Condition	Symbol	Min	Max	Units
Time bus must be free before a new transition can start	t _{BUF}	4.7	–	μs
Clock/data fall time	t _F	–	300	ns
Clock/data rise time	t _R	–	1,000	ns
Data hold time	t _{HD:DAT}	300	–	ns
Start condition hold time	t _{HD:STA}	4.0	–	μs
Clock HIGH period	t _{HIGH}	4.0	50	μs
Clock LOW period	t _{LOW}	4.7	–	μs
SCL clock frequency	f _{SCL}	–	400	kHz
Data setup time	t _{SU:DAT}	250	–	ns
Start condition setup time	t _{SU:STA}	4.7	–	μs
Stop condition setup time	t _{SU:STO}	4.0	–	μs
Clock frequency	f _{CK}	10	100	kHz

Serial Presence-Detect

Table 16: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage with temperature sensor option	VDDSPD	3.0	3.6	V
Input high voltage: Logic 1; All inputs	V _{IH}	2.1	VDDSPD + 0.5	V
Input low voltage: Logic 0; All inputs	V _{IL}	-0.6	0.8	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	-	0.4	V
SPD input leakage current: V _{IN} = GND to V _{DD}	I _{LI}	0.10	3.0	μA
SPD output leakage current: V _{OUT} = GND to V _{DD}	I _{LO}	0.05	3.0	μA
SPD standby current	I _{SB}	1.6	4.0	μA
Power supply current, READ: SCL clock frequency = 100 kHz	I _{CC_R}	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I _{CC_W}	2.0	3.0	mA
Average temperature sensor current	-	-	500	μA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3	-	μs	
Data-out hold time	t _{DH}	200	-	ns	
SDA and SCL fall time	t _F	-	300	ns	2
Data-in hold time	t _{HD:DAT}	0	-	μs	
Start condition hold time	t _{HD:STA}	0.6	-	μs	
Clock HIGH period	t _{HIGH}	0.6	-	μs	
Noise suppression time constant at SCL, SDA inputs	t _I	-	50	ns	
Clock LOW period	t _{LOW}	1.3	-	μs	
SDA and SCL rise time	t _R	-	0.3	μs	2
SCL clock frequency	f _{SCL}	-	400	kHz	
Data-in setup time	t _{SU:DAT}	100	-	ns	
Start condition setup time	t _{SU:STA}	0.6	-	μs	3
Stop condition setup time	t _{SU:STO}	0.6	-	μs	
WRITE cycle time	t _{WRC}	-	10	ms	4

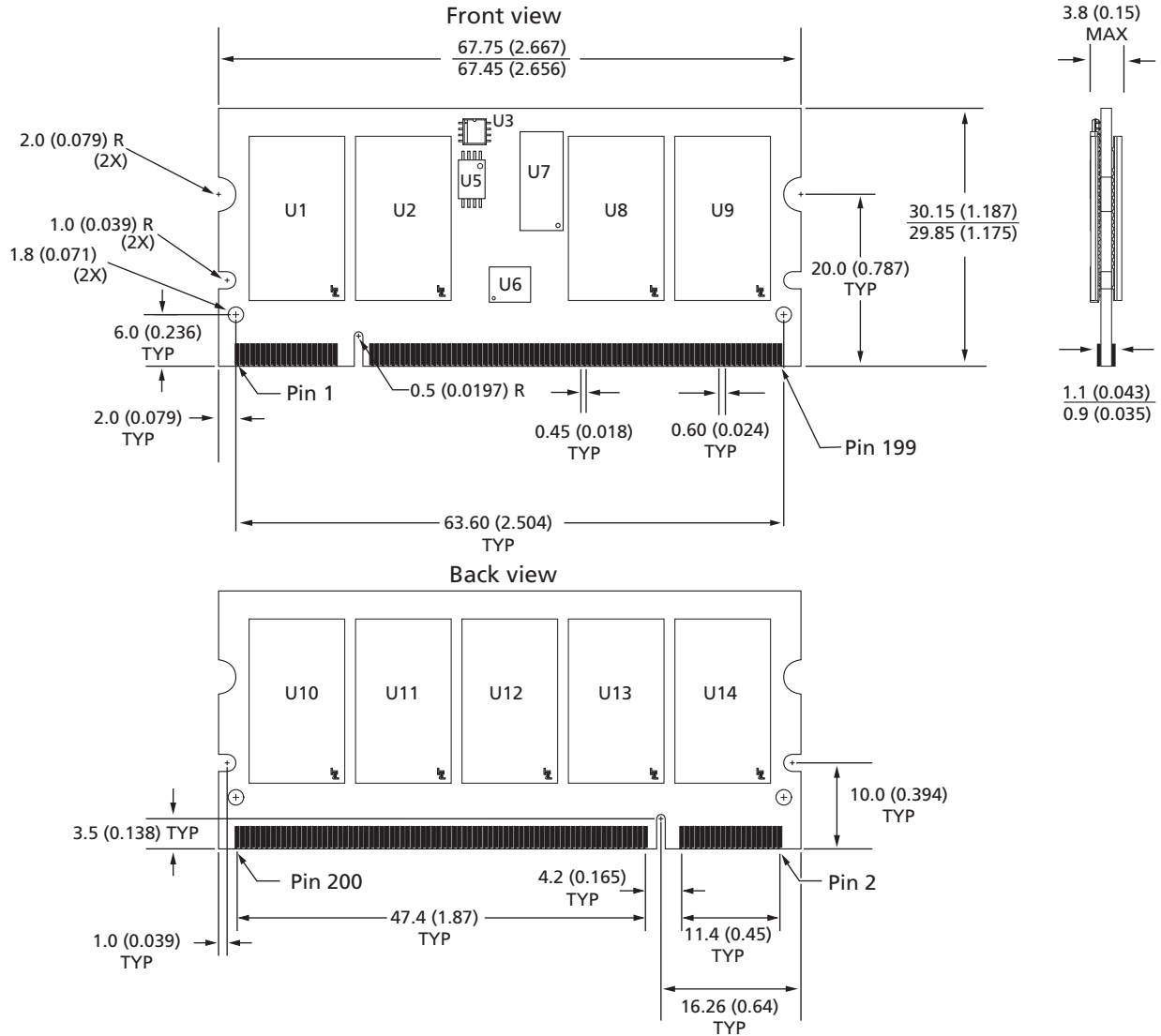
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD.

Module Dimensions

Figure 3: 200-Pin DDR2 SODIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.



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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.